Volume 2, Issue 6 June 2016 ISSN NO: 2454 - 7514

North Asian International Research Journal Consortium

North Asian International Research Journal Of Science, Engineering and Information Technology

IRJIF IMPACT FACTOR: 3.01

NAIRJC JOURNAL PUBLICATION

North Asian International Research Journal Consortium

Welcome to NAIRJC

ISSN NO: 2454 -7514

North Asian International Research Journal of Science, Engineering & Information Technology is a research journal, published monthly in English, Hindi. All research papers submitted to the journal will be double-blind peer reviewed referred by members of the editorial board. Readers will include investigator in Universities, Research Institutes Government and Industry with research interest in the general subjects

Editorial Board

Address: - Dr. Ashak Hussain Malik House No. 221 Gangoo, Pulwama, Jammu and Kashmir, India - 192301, Cell: 09086405302, 09906662570, Ph. No: 01933-212815,
Email: nairjc5@gmail.com, nairjc@nairjc.com, info@nairjc.com Website: www.nairjc.com

Enhanced AHB for audio codec control using I2C

G.S.ARUNKUMAR [1], N.SOUNDAR [2], MATHANKUMAR [3] & VIVEKKUMAR [4]

[1] Assistant Professor (ECE), Sri Eshwar College of Engineering, Coimbatore.
[2] PG Scholar (VLSI Design), Sri Eshwar College of Engineering, Coimbatore.
[3] Testing engineer and TL, Success Solution, Coimbatore.
[4] Assistant Professor (ECE), Sri Eshwar College of Engineering, Coimbatore.

Abstract— ***An enhanced AHB for audio codec control is a typical System-on-Chip (SOC) design is having many different cores linked together with complex on chip bus communication architectures. This on-chip bus communication architecture determines how these different functional cores exchange and synchronize their data. AMBA has a hierarchy of buses with Advance high performance bus (AHB) that can be used to get connected to high performance peripherals and APB (Advance Peripheral Bus) that can be connected to low performance peripherals. Inter integrated circuit (I2C) is a multi-master, multi-slave, single-ended, serial computer bus. AHB master is the main component that initiates the read and writes transactions. This paper focuses on design of enhanced AHB for audio codec control using I2C.***

Keywords- ***I2C, AMBA, AHB, APB, AHB Master, SOC, Split transaction.***

1. INTRODUCTION

The Advanced Microcontroller Bus Architecture specification is an on-chip communication standard for designing high-performance microcontrollers. A typical System-on-Chip (SOC) design contains many different IP cores linked together with sophisticated on-chip bus communication architectures. This deals with a great impact on the system's performance. There are many communication architectures used in the industry like AMBA, PI-bus, Core Connect, Wishbone, Avalon etc. AMBA is a standard interface specification which makes sure of the compatibility between different IP components provided by different design vendors.

1.1 I2C

The I2C bus was designed by Philips in the early '80s to allow easy communication between components which reside on the same circuit board. Philips Semiconductors migrated to NXP in 2006.

The name I2C translates into "Inter IC". Sometimes the bus is called IIC or I²C bus.

The original communication speed was defined with a maximum of 100 Kbit per second and many applications don't require faster transmissions. For those that do there is a 400 Kbit fast mode and – since 1998 – a high speed 3.4 Mbit option available. Recently, *fast mode plus* a transfer rate between this has been specified. Beyond this, there is the ultra fast mode UFM, but it frankly is no real I2C bus.

I2C is not only used on single boards but also to connect components which are linked via cable. Simplicity and flexibility are key characteristics that make this bus attractive to many applications.

1.2 TYPES OF BUSES

AMBA 2.0 specification defines three different buses [1]:-

1. Advanced high Performance Bus (AHB)
2. Advanced System Bus (ASB)
3. Advanced Peripheral Bus

An AMBA based embedded microcontroller typically consists of a high-performance system backbone bus (AMBA AHB or ASB), which is able to maintain the external memory bandwidth. AHB bus provides a high-bandwidth interface between different elements which are involved in the different transfers.

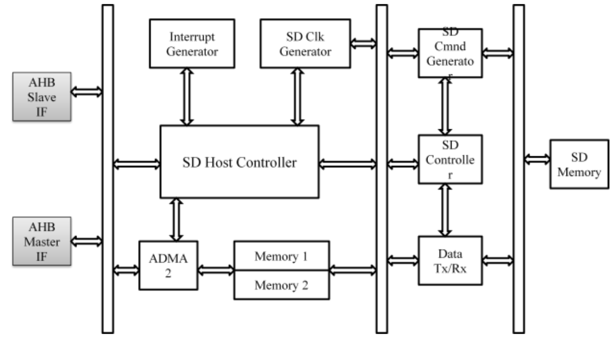

Fig.1 Block Diagram of SD Host controller

There is also an availability of the AHB to APB Bridge, which is used to access low peripheral devices on high performance bus. APB Bridge is only the master for APB bus [2]. This paper mainly deals with AMBA AHB bus and particularly AHB master.

The paper is divided into three sections. First section is introduction that introduces AHB system, its features and some signals associated with AHB master. Second section has the description related to finite state machine designed for AHB master. Finally the Third section contains the results of implementing the state machine in the Verilog hardware description language.

1.2.1. Advanced high Performance Bus (AHB)

AHB bus is a new generation of AMBA 2.0 specification which is intended to point out the requirements of high-performance synthesizable designs. AHB is the new level of bus which sits above ASB and APB. The features required for high performance, high clock frequency systems are as follows [1]:-

- Burst transfers (4/8/16 beat burst)
- Split transactions
- Bus master handover in single cycle
- Single clock edge operation
- Wider data bus configuration (8/16/32/64/128/256/512/1024 bits)
- Pipelined operation

An AMBA AHB design consists of one or more bus masters (AHB supports up to 16 masters), typically a system might contain at least the processor as an AHB master. However, DMA (Direct Memory Access) or DSP (Digital Signal Processor) can also be used as bus masters. The external memory interfaces like SRAM, ROM, APB Bridge and different internal memories are the common AHB slaves. Any other peripherals in the system might also be included as AHB slaves. An AHB bus master has complex interface in AMBA and can initiate read/write operations by providing an address and control information in first clock cycle. Only one bus master at one time is allowed to transfer the data on the bus and this decision is made by an Arbiter in the system. An arbiter plays a very important role in resource sharing. Arbiter may take this decision of granting access the bus to any particular master based on different arbitration schemes like priority wise or round robin etc. A bus slave responds to an operation within a given address space range provided by master. The bus slave signals back to the active master regarding the success or failure of the data transfer [3].

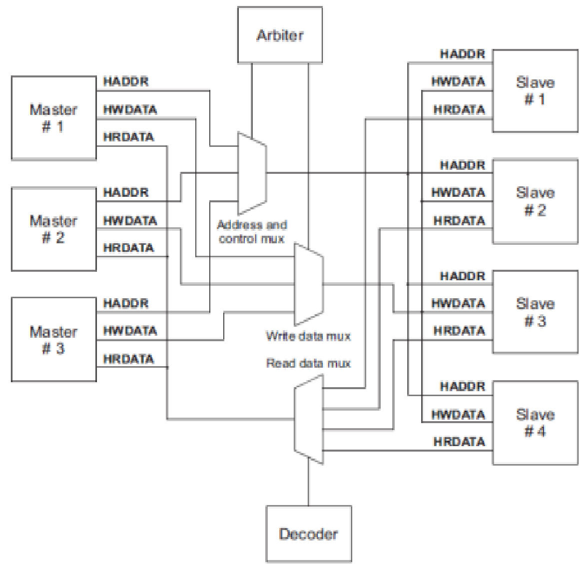

Fig.2AHB multiplexer interconnection [1]

1.2.2 AHB Operation

Before starting the AMBA AHB transfer, the bus master must have to be granted access to the bus. In this process first of all master asserts a request signal to an arbiter. Now the arbiter will indicate when the master will get the grant of the bus. This decision of granting the access to bus is achieved using some arbitration mechanism like priority based or round robin mechanism etc. A granted bus master then starts the AHB transfer by first driving an address and control signals.

These address and control signals provide information about an address, direction and width of the transfer, burst transfer information if the transfer forms the part of the burst [1].

There are two different forms of burst transfers that are allowed [1]:-

- INCREMENTING: does not wrap at address boundaries
- WRAPPING: wrap at address boundaries

Every transfer consists of two phases as:-

- Address and control cycle phase
- Data phase

The address phase can't be extended and so the slaves has to sample the address and control signals during this phase only. But the data phase can be extended using HREADY signal, HREADY = LOW inserts wait states in between transfer and HREADY = HIGH indicates the completion of the transfer. In normal operation a master is allowed to complete all the data transfers in a particular burst before an arbiter grants the access of bus to another master [1]. Different signals used by AHB masters are shown in figure 3 as follows:

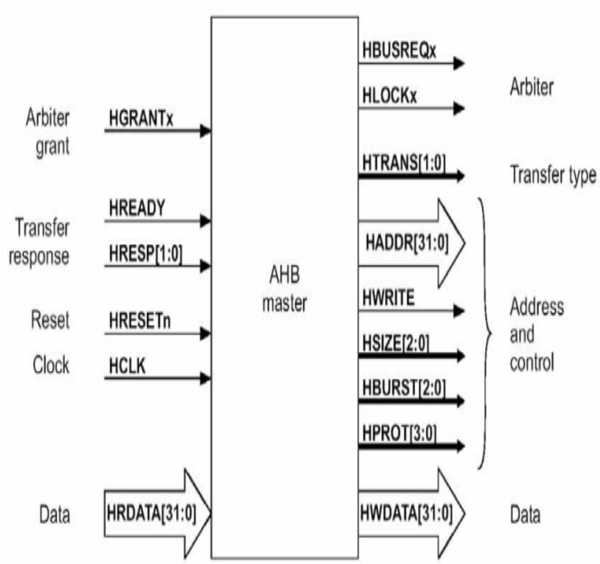

Fig.3 AHB master interface [2]

2. FINITE STATE MACHINE FOR AHB MASTER

Main component in the AMBA system is the master with complex interface that can initiate the read or write transfer to any slave. So it is imperative that master is properly designed for an AHB system to work. In addition AHB master implementation has to support advance features like burst transfers, split transaction, pipelined operation as defined in the specification.

The following section contains the brief description of every state in the diagram.

1) IDLE: FSM of AHB master starts with IDLE state and this is the default state in the state machine. When master has no data to transfer or it has just finished the transaction at that time it will stay in this IDLE state. When master wants to perform another transaction then it will have to request for a bus to an arbiter so it will move in to BUSREQ state.

2) BUSREQ: (Bus Request) The AHB master will wait in this state until the bus has been granted by an AHB arbiter. Arbiter grants the access to bus using some arbitration mechanism. Once the bus is granted to that particular master then it will move to NSEQRD state for the read transfer or to NSEQWR state for write transfer.

3) NSEQRD: (Non Sequential Read) As we earlier studied that AMBA AHB has the pipelined

architecture, so address and control information is sent first in this cycle and based on the control information like burst size (hburst) and size of transfer (hsize) , next state and address are decided. If the transfer type is a single burst transfer then next state will be RDWAIT for getting data for this address provided by the master in first cycle and if the transfer type is an incrementing burst transfer then the next state will be SEQRD. If in between the grant to the master is lost due to some reason then it will move to LASTRD state for latching data and freeing the bus. In this state, it is a single transfer or a first transfer of a burst so htrans value will be „10" which shows non sequential transfer.

4) SEQRD: (Sequential Read) this is a sequential transfer, the value for htrans will be "11" which shows sequential transfer type. The next address will be generated based on the size of the transfer (8/16/32/64 bits etc). AMBA AHB is a byte addressable i.e. each address contains 1 byte.

If the size is byte (8 bits), then previous address will be incremented by 1, if it is half word then previous address will be incremented by 2 and for word the previous address will be incremented by 4. Based on the value of hburst (4/8/16 beat burst), burst complete signal is asserted to show that this is the last transfer on the burst and state is transferred to RDWAIT to latch the final data of the burst. If grant is lost in the middle of the burst due to some reason then state will be transited to LASTRD and then master will re arbitrate for the bus for the completion the remaining burst.

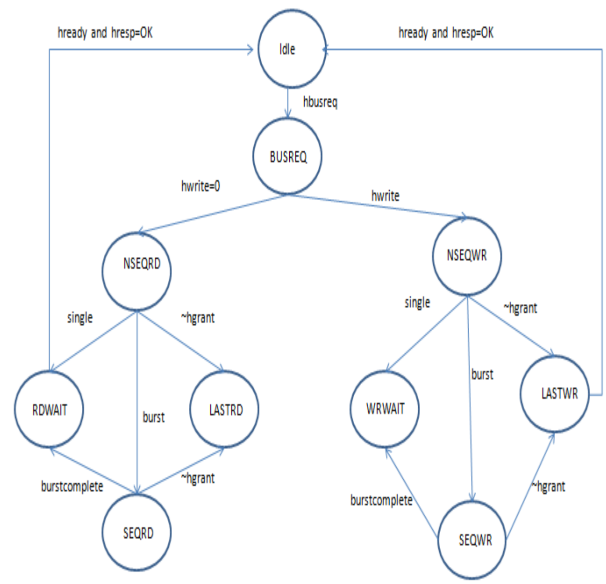

Fig.4 FSM of AHB Master

5) RDWAIT: (Read Wait) The master will be in this state if it is a single transfer or the last transfer of the burst. The final data is latched in this state and if hready = high and OK response is asserted by the slave, it shows that the read transaction has finished successfully on the bus and master can move to IDLE state.

6) LASTRD: (Last Read) The master will go in this state when it lost the grant of the bus in the middle of the transaction. Then in this state it will latch the data of the address transferred in the previous cycle due to pipelining and then re-arbitrate master for the bus, for the completion of the remaining burst.

7) NSEQWR: (Non Sequential Write) In this state of FSM, hwrite signal will be 1 to indicate the write transaction from the master. If it is a single burst write transfer then next state will be WRWAIT for transferring data for this address provided by the master and if it is incrementing burst transfer then the next state will be SEQWR. If grant to the master is lost in the middle of the transfer due to some reason then it will move to LASTWR state for writing the last data and freeing bus. In this state, it is a single transfer or a first transfer of a burst, so htrans value will be "10" which shows non sequential transfer.

8) SEQWR: (Sequential Write) This state indicates the sequential transfer, now the value for htrans will be "11" which shows sequential transfer. The next address will be generated based on the size of the transfer (8/16/32/64 bits etc). If the size is byte, then previous address will be incremented by 1, If the size is half word then previous address will be incremented by 2 and if word then previous address will be incremented by 4. Based on the value of hburst (4/8/16 beat burst), the burst complete signal is asserted to show that this is the last transfer on the burst and state is transferred to WRWAIT to write the final data of the burst. If grant is lost in the middle of the burst transfer then state will be transited to LASTWR and then master will re arbitrate for access to bus for the completion of remaining burst.

9) WRWAIT: (Write Wait) Master will be in this state, when it is a single transfer or the last transfer of the burst. The final data is written in this state and if hready = high and OK response is asserted by the slave, indicating that the write transaction has finished successfully on the bus and master can move to the IDLE state.

10) LASTWR: (Last Write) The master will be in this state if it lost the grant of the bus in the middle of the transfer, so in this state it will write the data of the address in the previous cycle due to pipeline operation and then master will re-arbitrate for the bus for the completion of the remaining burst. If in the middle of the transaction, error, split or retry response comes from the slave then master will stop the transaction and move to the IDLE state.

3. RESULTS AND PERFORMANCE ANALYSIS

After the completion of this finite state machine, any hardware description language can be used to implement it and checked for functionality correctness. In this Paper, the state machine is implemented in Verilog HDL language and XILINX simulation tool is used to simulate the design and generate the waveforms.

The Figure 5 as shown below indicates single burst write transfer operation with size of the transfer equal to 32 bit. When the request is granted to the master, starts the transaction by giving address and the control information. The value of hburst = 000, indicates single burst transfer and hwrite = 1 indicates write transfer. htrans value is 10 for the transfer indicating non sequential transfer. Hresp = 00, indicates OK response from the slave showing slave is ready to receive data. Hsize = 010 indicating word transfer.

The Figure 6 and 7 provides the RTL schematic and Power analysis of FIFO in AMBA AHB Implementation.

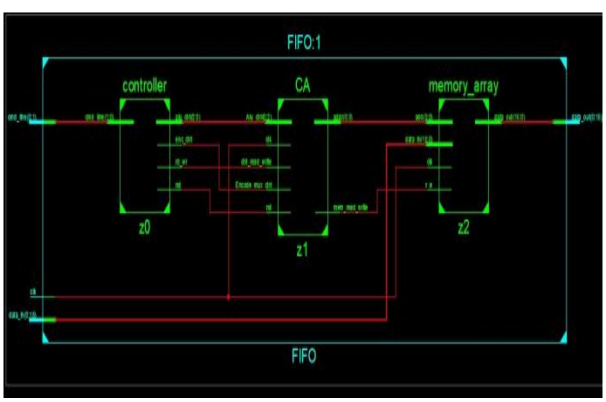

Fig .6 RTL Schematic of FIFO

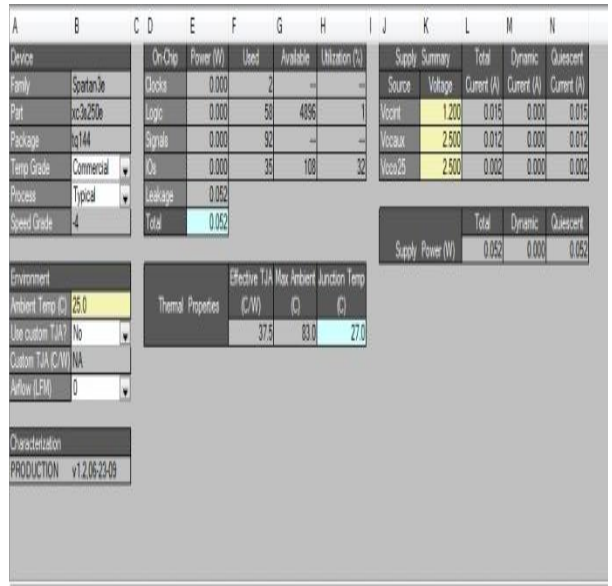

Fig .7 Power analysis of FIFO

This verilog coding is compiled in ALTERA QUARTUS II and communication software Nios II is used for interlink of hardware and QUARTUS II software.

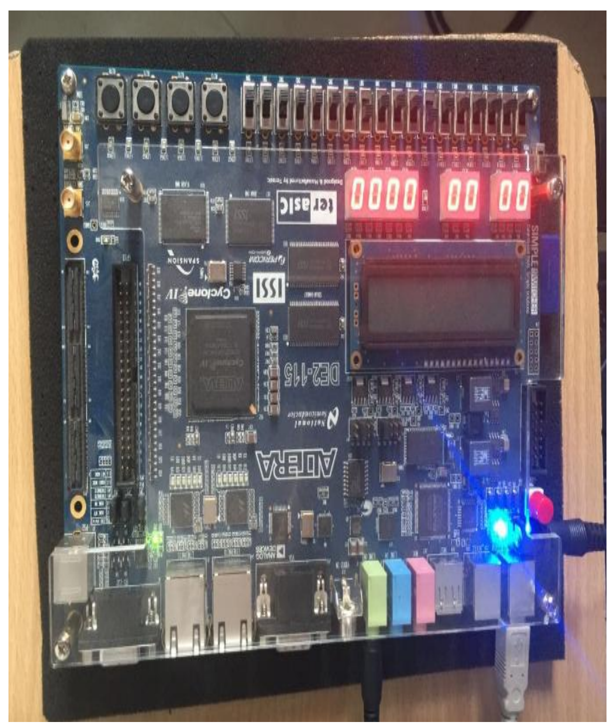

Fig: 8 ALTERA QUARTUS II hardware output.

CONCLUSION

The efficient FSM design for AMBA AHB master circuit has been successfully simulated using Xilinx and Modelsim tools. AMBA master is the main integral part of the system. Hardware and simulation results using ALTERA QUARTUS II has been shown that an enhanced design for audio codec control is designed using I2C.

REFERENCES

[1] AMBA Specification Rev 2.0. ARM Ltd., 1999.

[2] “AMBA Design Kit revision r3p0”, Technical Reference Manual, ARM Inc.

[3] “AHB Example AMBA System”, Technical Reference Manual, ARM Inc.

[4] Rohit Hardia, Prof.Jai Karan Singh, Prof..Mukesh Tiwari “ Design And Simulation of a typical high performance AHB Reconfigurable Master For On-chip bus Architecture using Verilog HDL”, International Conference on Communication Systems and Network Technologies, IEEE 2011.

[5] Priyanka Gandhani, Charu Patel “Moving from AMBA AHB to AXI Bus in SoC Designs: A Comparative Study”, 2011.

Publish Research Article

Dear Sir/Mam,

We invite unpublished Research Paper,Summary of Research Project,Theses,Books and Book Review for publication.

Address:- Dr. Ashak Hussain Malik House No-221, Gangoo Pulwama - 192301
Jammu & Kashmir, India
Cell: 09086405302, 09906662570,
Ph No: 01933212815
Email:- nairjc5@gmail.com, nairjc@nairjc.com , info@nairjc.com
Website: www.nairjc.com