Volume 2, Issue 3 March 2016 ISSN NO: 2454 - 7514

North Asian International Research Journal Consortium

North Asian International Research Journal

Of

Science, Engineering and Information Technology

IRJIF IMPACT FACTOR: 3.01

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ISSN NO: 2454 -7514

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Address: - Dr. Ashak Hussain Malik House No. 221 Gangoo, Pulwama, Jammu and Kashmir, India - 192301, Cell: 09086405302, 09906662570, Ph. No: 01933-212815,
Email: nairjc5@gmail.com, nairjc@nairjc.com, info@nairjc.com Website: www.nairjc.com

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HYBRID SELF ORGANIZATION BASED DATA ENCODING FOR REDUCING ENERGY CONSUMPTION IN NOC

AMANDEEP KAUSHAL [1] & SARABDEEP SINGH [2]

[1](E.C.E, Chandigarh Engineering College, India)

[2](Asst. Prof., E.C.E, Chandigarh Engineering College, India)

ABSTRACT

Network-on-chip is a very active research field with many practical applications in industry. The major goal of communication-centric design and NoC paradigm is to achieve greater design productivity and performance by handling the increasing parallelism, manufacturing complexity, wiring problems, and reliability. The NoC architecture uses layered protocols and packet-switched networks which consist of on-chip routers, links, and network interfaces on a predefined topology. As technology shrinks, the power dissipated by the links of a network-on-chip (NoC) starts to compete with the power dissipated by the other elements of the communication subsystem, namely, the routers and the network interfaces (NIs).

Index Terms— Coupling switching activity, data encoding, interconnection on chip, low power, network-on-chip (NoC), power analysis.

I. INTRODUCTION

In this paper, we focus on techniques aimed at reducing the power dissipated by the network links. In fact, the power dissipated by the network links is as relevant as that dissipated by routers and network interfaces (NIs) and their contribution is expected to increase as technology scales [5]. In particular, we present a set of data encoding schemes operating at flit level and on an end-to-end basis, which allows us to mini-mize both the switching activity and the coupling switching activity on links of the routing paths traversed by the packets. The proposed encoding schemes, which are transparent with respect to the router implementation, are presented and dis-cussed at both the algorithmic level and the architectural level, and assessed by means of simulation on synthetic and real traffic scenarios. The analysis takes into account several aspects and real traffic scenarios. The analysis takes into account several aspects and metrics of the design, including silicon area, power dissipation, and energy consumption. Nowadays, the on-chip communication issues are as relevant as, and in some cases more relevant than, the computation-related issues [4]. In fact, the communication subsystem increasingly impacts the traditional design objectives, including cost (i.e., silicon area), performance, power dissipation, energy consumption, reliability, etc. As technology shrinks, an ever more significant fraction of the total power budget of a complex many-core system-on-chip (SoC) is due to the communication subsystem.

II. NoC TOPOLOGIES

Topology is a very important feature in the design of NoC because design of a router depends upon it. Different topologies are proposed in the literature forth design of NoC. Commonly used topologies are mesh, ring, torus, binary tree, bus and spider on. Some researchers have also proposed topologies suitable for an application or an application area.

The topology is statically known and usually very regular (e.g., a mesh)

(i) Mesh: A mesh-shaped network consists of m columns and n rows. The routers are situated in the intersections of two wires and the computational resources are near routers. Addresses of routers and resources can be easily defined as x-y coordinates in mesh. Regular mesh network is also called as Manhattan Streetnetwork.

(ii) Torus: A Torus network is an improved version of basic mesh network. A simple torus network is a mesh in which the heads of the columns are connected to the tails of the columns and the left sides of the rows are connected to the right sides of the rows. Torus network has better path diversity than mesh network, and it also has more minimal routes.

(iii) Tree: In a tree topology nodes are routers and leaves are computational resources .The routers above a leaf are called as leaf's ancestors and correspond the leafs below the ancestor are its children. In a fat tree topology each node has replicated ancestors which mean that there are many alternative routes between nodes.

(iv) Butterfly: A butterfly network is uni or bidirectional and butterfly-shaped network typically uses a deterministic routing. For example a simple unidirectional butterfly network contains 8 input ports, 8 output ports and 3 router levels which each contain 4 routers. Packets arriving to the inputs on the left side of the network are routed to the correct output on the right side of the network. In a bidirectional butterfly network, all the inputs and outputs are on the same side of the network. Packets coming to inputs are first routed to the other side of the network, then turned around and routed back to the correct output.

(v) Polygon: The simplest polygon network is a circular network where packets travel in loop from router to other Network becomes more diverse when chords. Butterfly network with 4 inputs, 4 outputs and 2 router stages each containing 2 routers. When there are chords only between opposite routers, the topology is called as spidergon .Polygon (hexagon) network with all potential chords.

(vi) Star: A star network consists of a central router in the middle of the star, and computational resources or subnet works in the spikes of the star. The capacity requirements of the central router are quite large, because all the traffic between the spikes goes through the central router. That causes a remarkable possibility of congestion in the middle of the star.

(vii) Double chain topology: A new class of interconnection network topologies, the double- chain NoC topology. Double-chain topologies are comprised of two disjoint but overlapping chains, each of which connects all network nodes. These topologies are well suited to both 2-D planar VLSI technology and the ABC router

micro architecture. Double-chain topologies provide an advantage over 2-D Mesh networks for ABC routers by providing two paths comprised solely of "straight-path" links between all source-destination pairs. Double-chain topologies also offer higher amount of path diversity as compared to a standard2-D Mesh. In contrast to a 2-D Mesh, where all source and destination pairs have only two deadlock-free paths between them, double-chain topologies offer four such paths.

B.NoC Router: A router is a device that forwards data packets between computer networks, creating an overlay internetwork. A router is connected to two or more data lines from different networks. When a data packet comes in one of the lines, the router reads the address information in the packet to determine its ultimate destination. Then, using information in its routing table or routing policy, it directs the packet to the next network on its journey. Routers perform the "traffic directing" functions on the Internet. A data packet is typically forwarded from one router to another through the networks that constitute the internetwork until it gets to its destination nodes a Routing: Arbitration and routing logic are designed for minimal complexity and low latency, because router stages typically must take no more than a few cycles.

III. CLASSIFICATION OF ROUTING IN NoC:

(i) Deterministic Vs Adaptive Routing: There are many ways to classify routing in NoC One way to classify routing in NoC could be deterministic or adaptive. In deterministic routing the path from the source to the destination is completely determined in advance by the source and the destination addresses. In adaptive routing, multiple paths from the source to the destination are possible. When a packet enters a router, destination address is read from the header and accordingly, the routing function computes all possible output ports where this packet can be forwarded to, Then a routing function selects one of the admissible output ports to forward the packet. The selectivity of output port depends upon the dynamic network conditions such as congestion and link faults. There also exist partially adaptive routing algorithms which restrict certain paths for communication. They are simple and easy to implement compared to adaptive routing algorithms.

(ii) Minimal and Non-Minimal Routing: A routing which uses shortest possible paths for communication is known as minimal routing. It is also possible to use longer paths for data transfer from source to destination. This possibility results from the adaptively offered by a routing algorithm. The type of routing which uses longer paths for communication although shortest paths do exist is known as non-minimal routing. Non-minimal routing has some advantages over minimal routing including possibility of balancing network load and fault tolerance.

(iii) Static and Dynamic Routing: In static routing, the path cannot be changed after a packet leaves the source. In dynamic routing, a path can be altered any time depending upon the network conditions. Source routing is static while distributed routing can be static or dynamic depending upon the routing algorithm used. It should be noted that even when adaptive routing algorithms are used to compute paths for source routing, it remains static unless some sophisticated selection technique is introduced in the network.

(iv) Application Specific Routing: This type of routing is used for specialized applications or a set of concurrent applications. For a specific application of NoC based SoC in embedded systems we can have a good profile of the communications among different cores. This means that it is possible to know that which cores are communicating with each other and which cores do not communicate at all. In order to get best performance of NoC for specific application, we can have specialized application specific routing algorithm. APSRA is one such algorithm.

(v) Minimal Adaptive Routing: Minimal adaptive routing algorithm always routes packets along the shortest path. The algorithm is effective when more than one minimal or as short as possible, routes between sender and receiver exist. The algorithm uses route which is least congested.

(vi) Fully Adaptive Routing: Fully adaptive routing algorithm uses always a route which is not congested. The algorithm does not care although the route is not the shortest path between sender and receiver. Typically an adaptive routing algorithm sets alternative congestion free routes to order of superiority. The shortest route is the best one.

(vii) Congestion Look Ahead: A congestion look ahead algorithm gets information about blocks from other routers. On the grounds of this information the routing algorithm can direct packets to bypass the congestions.

(viii) Turnaround Routing: Turnaround routing is a routing algorithm for butterfly and fat-tree networks. Senders and receivers of packets are all on the same side of the network. Packets are first routed from sender to some random intermediate node on the other side of the network. In this node the packets are turned around and then routed to the destination on the same side of the network, where the whole routing started .The routing from the intermediate node to the definite receiver is done with the destination-tag routing. Routers in turnaround routing are bidirectional which means that packets can flow through router in both forward and backward directions. The algorithm is deadlock-free because packets only turn around once from a forward channel to a backward channel. SPIN (Scalable Programmable Interconnect Network) is a fat-tree shaped network which uses turnaround routing algorithm. In fault-tolerant XGFT system (extended Generalized Fat Tree) the turnaround routing is called as turn back routing. The network topology in XGFT systems is also fat-tree. XGFT's turn back routing slightly differs from the basic turn around algorithm. While traditional turnaround routing chooses the intermediate node randomly, the XGFT's turn back algorithm can choose it by itself. This is useful when the network is congested.

(ix) Turn-Back-When-Possible: Turn-back-when-possible (TBWP) is an algorithm for routing on tree networks. It is a little bit improved version of the turnaround routing. When turn-back channels are busy, the algorithm looks for free routing path on a higher switch level. A turn-back channel is a channel between a forward and a backward channel. It is used to change the routing direction in the network.

(x) Odd-Even Routing: An odd-even routing is an adaptive algorithm used in dynamically adaptive and deterministic (DyAD) Network on Chip system. The odd-even routing is a deadlock free turn model which prohibits turns from east to north and from east to south at tiles located in even columns and turns from north to

west and south to west at tiles located in odd columns. The DyAD system uses the minimal odd-even routing which reduces energy consumption and also removes the possibility of live lock.

(xi) XY Routing Algorithm: It is one of the simplest and most commonly used routing algorithms used in NoC. It is a static, deterministic and deadlock free routing algorithm. Out of eight possible turns in mesh topology, XY routing algorithm allows half the turns by restricting rest of the half. According to this algorithm, a packet must always be routed along horizontal or X axis of mesh until it reaches the same column as that of destina Then it should be routed along vertical or Y axis and towards the location of destination resource.

IV. RELATED WORKS AND CONTRIBUTIONS

In the next several years, the availability of chips with 1000 cores is foreseen [6]. In these chips, a significant fraction of the total system power budget is dissipated by interconnection networks. Therefore, the design of power-efficient interconnection networks has been the focus of many works published in the literature dealing with NoC architectures. These works concentrate on different components of the interconnection networks such as routers, NIs, and links. Since the focus of this paper is on reducing the power dissipated by the links, in this section, we briefly review some of the works in the area of link power reduction. These include the techniques that make use of shielding [7], [8], increasing line-to-line spacing [9], [10], and repeater insertion [11]. They all increase the chip area. The data encoding scheme is another method that was employed to reduce the link power dissipation. The data encoding techniques may be classified into two categories. In the first category, encoding techniques concentrate on lowering the power due to self-switching activity of individual bus lines while ignoring the power dissipation owing to their coupling switching activity. In this category, bus invert (BI) [12] and INC-XOR [13] have been proposed for the case that random data patterns are transmitted via these lines. On the other hand, gray code [14], T0 [15], working-zone encoding [16], and T0-XOR [17] were suggested for the case of correlated data patterns. Application-specific approaches have also been proposed [18]–[22]. This category of encoding is not suitable to be applied in the deep submicronmeter technology nodes where the coupling capacitance constitutes a major part of the total interconnect capacitance. This causes the power consumption due to the coupling switching activity to become a large fraction of the total link power consumption, making the aforementioned techniques, which ignore such contributions, inefficient [23]. The works in the second category concentrate on reduc-ing power dissipation through the reduction of the coupling switching [10], [22]–[30]. Among these schemes [10], [24]– [28], the switching activity is reduced using many extra control lines. For example, the data bus width grows from 32 to 55 in [24]. The techniques proposed in [29] and [30] have a smaller number of control lines but the complexity of their decoding logic is high. The technique described in [29] is as follows: first, the data are both odd inverted and even inverted, and then transmission is performed using the kind of inversion which reduces more the switching activity. In [30], the coupling switching activity is reduced up to 39%. In this paper, compared to [30], we use a simpler decoder while achieving a higher activity reduction.

VI. PROPOSED WORK

Basically we have processed with partial data encoding process which is optimized on the bases of dynamic tradeoff which provides reduction of delay and overall performance of the network on chip power reduction process with respect to completion time. The percentage increase of completion time is defined as the percentage increase of the time needed to drain a given amount of traffic. Structure based on data address buses, dynamic encoding techniques is modified and applied to lists which are self organizing or manually driven by given instruction set. A Hybrid structure for encoding technique is proposed for providing support to multiplexed address buses with reduction in power nearly around 49%. Overall performance of the network on chip is shown as 252% and delay with 200%. As the tolerance of the power dissipation in the communication process, 52% is the overall power reduction which is shown by the proposed work.

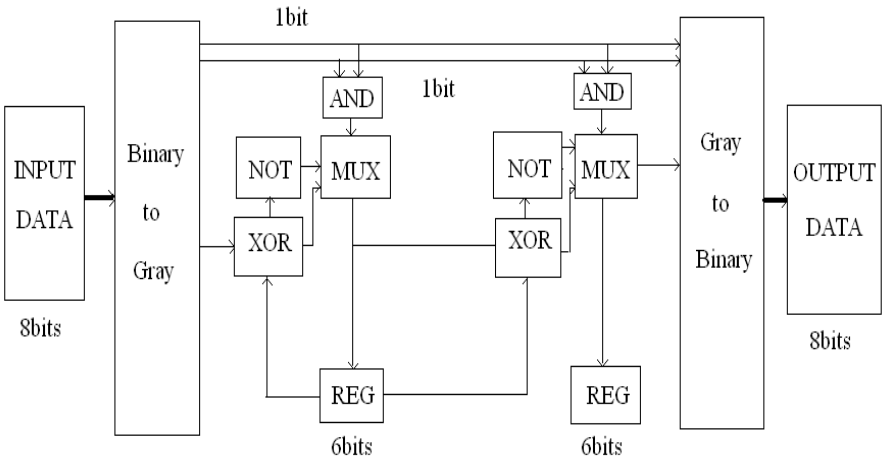

Figure 1: Shows the block diagram of the proposed architecture

VII. DATA FLOW DIAGRAMS FOR NOC PROJECT

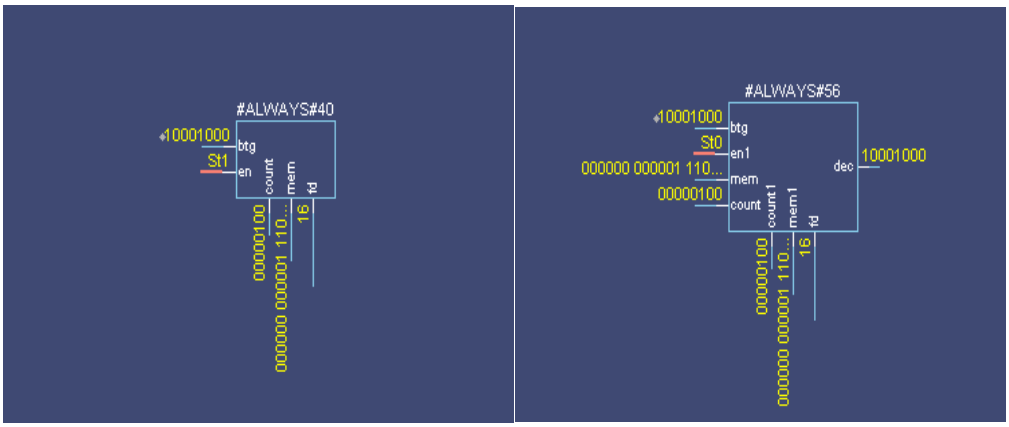

Figure 2: (a) on left shows the datapin for block 1 and (b) on right shows the datapin of block 2

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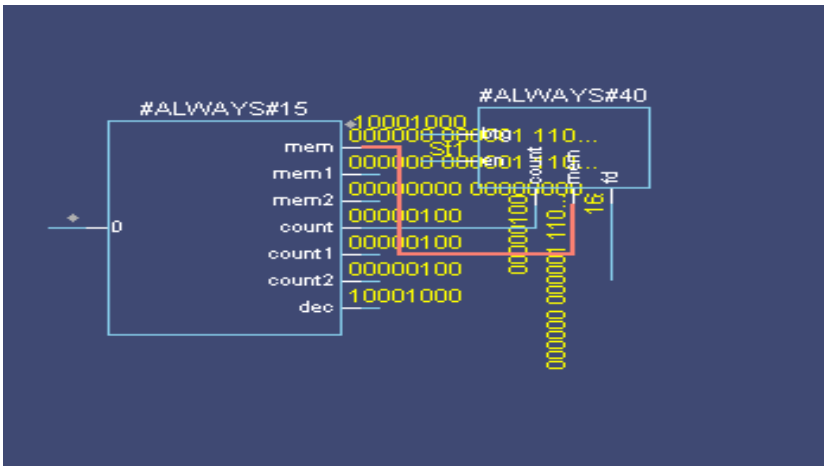

Figure 3: shows the input datapin diagram for the system

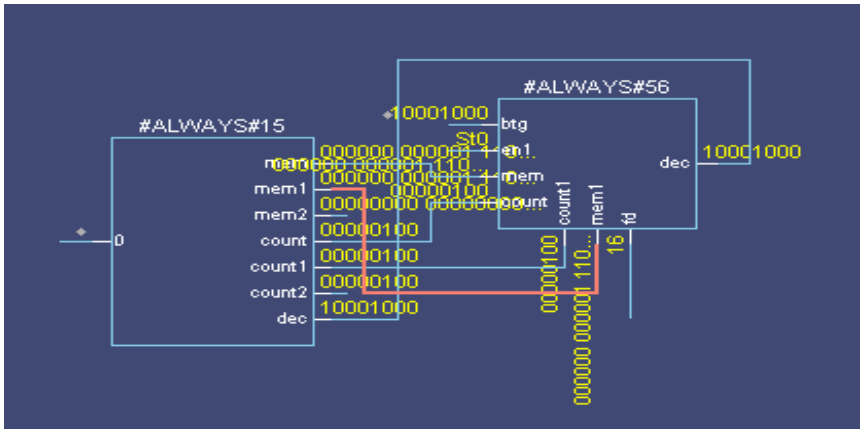

Figure 4: shows the data encoded by the encoding block

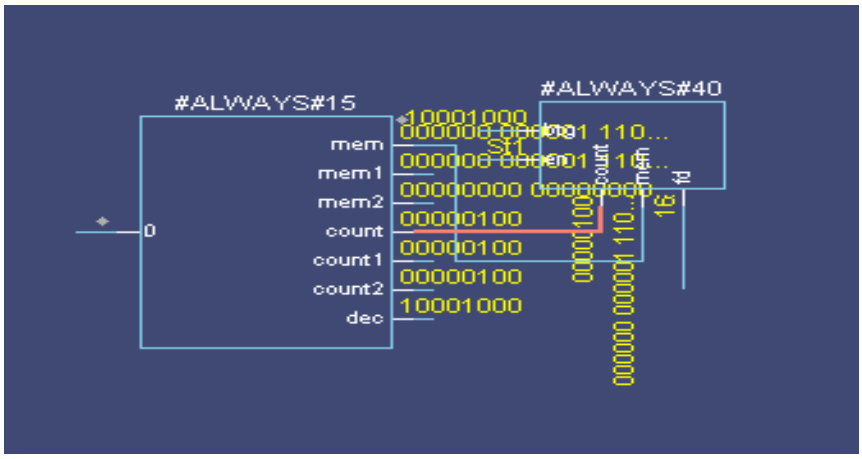

Figure 5: shows the data encoded by the encoding block

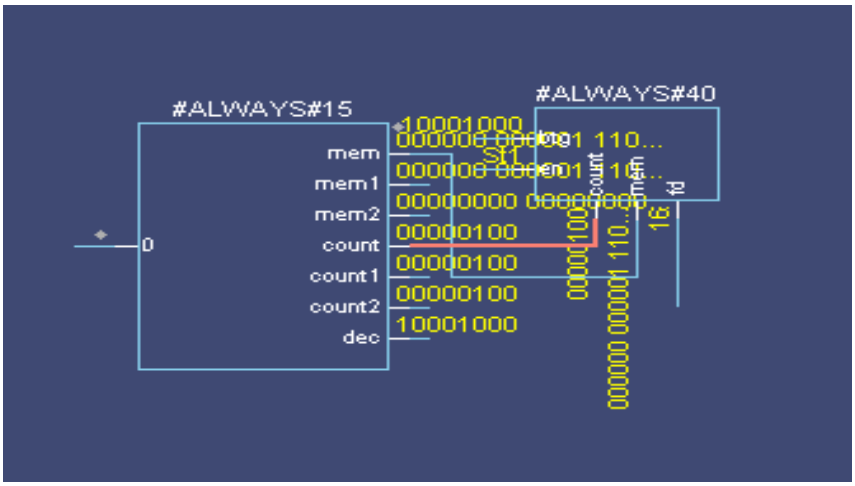

Figure 6: shows the data from the counter block

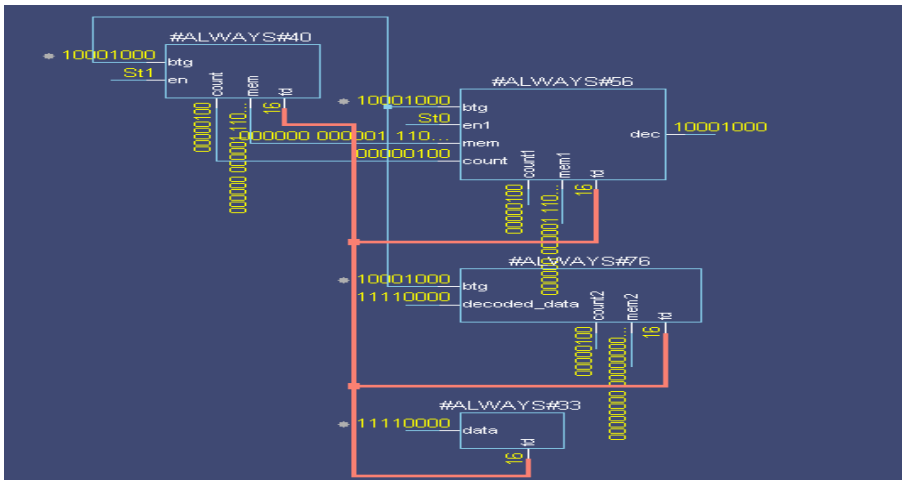

Figure 7: shows the networking block interface for main block

VIII. CONCLUSION

Basically we have processed with partial data encoding process which is optimized on the bases of dynamic trade off which provides reduction of delay and overall performance of the network on chip power reduction process with respect to completion time. The percentage increase of completion time is defined as the percentage increase of the time needed to drain a given amount of traffic. Structure based on data address buses, dynamic encoding techniques is modified and applied to lists which are self organizing or manually driven by given instruction set. A Hybrid structure for encoding technique is proposed for providing support to multiplexed address buses with reduction in power nearly around 49%. Overall performance of the network on chip is shown as 252% and delay with 200%. As the tolerance of the power dissipation in the communication process, 52% is the overall power reduction which is shown by the proposed work.

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